**What is claimed is:**

1. A flat panel display comprising a plurality of pixels, each pixel including at least a first transistor and a second transistor, wherein a semiconductor layer of the first transistor has a mobility which is different from a semiconductor layer of the second transistor.

2. The flat panel display according to claim 1, wherein the semiconductor layer of the first transistor has different grain size than the semiconductor layer of the second transistor.

3. The flat panel display according to claim 1, wherein the semiconductor layer of the first transistor has a lower mobility than the semiconductor layer of the second transistor

4. The flat panel display according to claim 3, wherein the semiconductor layer of the first transistor has a grain size that is about 10 times or more smaller than the semiconductor layer of the second transistor.

5. The flat panel display according to claim 1, wherein each of the pixels further comprises a luminescent device, the first transistor is a driving transistor and the second transistor is a switching transistor, wherein the switching transistor transmits data signals according to scan signals and the driving transistor drives the luminescent device so that an amount of current corresponding to the data signals is flown through the luminescent device, and the mobility of the semiconductor layer of the driving transistor is lower than the mobility of the semiconductor layer of the switching transistor.

6. The flat panel display according to claim 1, wherein the semiconductor layer of the first transistor comprises an amorphous silicon film, and the semiconductor layer of the second transistor is comprised of a polysilicon film.

7. The flat panel display according to claim 6, wherein the semiconductor layer of the first transistor further comprises polysilicon film, and the polysilicon film included in the semiconductor layer of the first transistor is a MILC (metal induced lateral crystallization) region.

8. The flat panel display according to claim 1, wherein the semiconductor layer of the first transistor includes a MILC (metal induced lateral crystallization) region and the semiconductor layer of the second transistor includes a MIC (metal induced crystallization) region.

9. A flat panel display comprising a plurality of pixels, each of the pixels including a first transistor and a second transistor, wherein a semiconductor layer of the first transistor has a crystal structure which is different from a crystal structure of the second transistor.

10. The flat panel display according to claim 9, wherein each of the pixels further comprises a luminescent device, the first transistor being is a driving transistor for driving the luminescent device and the second transistor is a switching transistor, wherein the switching transistor transmits data signals according to scan signals and the driving transistor for drives the luminescent device so that a certain amount of current is flown through the luminescent device according to the data signals, and the semiconductor layer of the driving transistor is comprised

of a polysilicon film having smaller grains than grains of the semiconductor layer of the switching transistor.

11. The flat panel display according to claim 10, wherein the semiconductor layer of the driving transistor has a grain size that is about 10 times or more smaller compared with the semiconductor layer of the switching transistor.

12. The flat panel display according to claim 9, wherein the semiconductor layer of the first transistor comprises an amorphous silicon film, and a semiconductor layer of the second transistor is comprised of a polysilicon film.

13. The flat panel display according to claim 12, wherein the semiconductor layer of the first transistor further comprises polysilicon film, and the polysilicon film included in the semiconductor layer is a MILC region.

14. The flat panel display according to claim 9, wherein a semiconductor layer of the first transistor includes a MILC region, and a semiconductor layer of the second transistor includes the MIC region.

15. A method for fabricating a flat panel display including at least a first transistor and a second transistor, comprising the steps of:

forming an amorphous silicon film on an insulating substrate;

crystallizing the amorphous silicon film into a polysilicon film that is divided into at least a first region having a first mobility and a second region having a second mobility; and

forming a semiconductor layer for the first transistor from the region with the first mobility and the second transistor from the region with the second mobility by patterning the polysilicon film, wherein the first mobility is different from the second mobility.

16. The method for fabricating a flat panel display according to claim 15, wherein the amorphous silicon film is crystallized through a SLS (sequential lateral solidification) crystallization process so that the semiconductor layer of the second transistor having a lower mobility than the semiconductor layer of the first transistor.

17. The method for fabricating a flat panel display according to claim 16, wherein the second transistor has a grain size that is about 10 times or more smaller than a grain size of the semiconductor layer of the second transistor having a higher mobility.

18. The method for fabricating a flat panel display according to claim 15, wherein the amorphous silicon film is crystallized by a MIC/MILC (metal induced crystallization/metal induced lateral crystallization) methods so that the semiconductor layer of the first transistor is crystallized by MIC and the semiconductor layer of the second transistor is crystallized by MILC, wherein the first transistor has a higher mobility than the second transistor.

19. A method for fabricating a flat panel display including a first transistor and a second transistor, the method comprising:

forming an amorphous silicon film on an insulating substrate;

crystallizing a part of the amorphous silicon film into a polysilicon film; and

forming a first semiconductor layer for the first transistor and a second semiconductor layer for the second transistor by patterning the polysilicon film and the amorphous silicon film, wherein the first semiconductor layer has a different mobility than the second semiconductor layer.

20. The method for fabricating a flat panel display according to claim 19, further comprising using the first semiconductor layer to fabricate the first transistor and the first semiconductor layer comprises the amorphous silicon film.

21 The method for fabricating a flat panel display according to claim 20, further comprising using the second semiconductor layer to fabricate the second transistor and the second semiconductor layer comprises at least a portion of the polysilicon film.

22. The method for fabricating a flat panel display according to claim 19, wherein the step of crystallization comprises crystallizing through SLS (sequential lateral solidification) crystallization only a portion of the amorphous silicon film into a polysilicon film while a portion of the amorphous silicon film is masked with a blocking layer, wherein the second semiconductor layer has a higher mobility than the first semiconductor layer and the second semiconductor layer is comprised of the polysilicon film, and the first semiconductor layer is comprised of the amorphous silicon film.

23. The method for fabricating a flat panel display according to claim 19, wherein the amorphous silicon film is crystallized through a MIC/MILC crystallization process using MILC masks having different widths, wherein the second semiconductor layer has a higher mobility than the first semiconductor layer.

24. The method for fabricating a flat panel display according to claim 23, wherein the step of crystallizing comprising crystallizing the second semiconductor layer by a MILC process, and crystallizing a portion of the first semiconductor layer by the MILC process to such that the first semiconductor layer includes a portion of the amorphous silicon film.

25. The method of claim 24, wherein a MILC mask covering the first semiconductor layer has a greater width than a MILC mask covering the second semiconductor layer.

26. The method for fabricating a flat panel display according to claim 23, wherein a degree in which the second semiconductor layer of the transistor having a lower mobility is crystallized by MILC is determined by width of the MILC mask, MILC crystallization time and crystallization temperature.

27. A flat panel display comprising R, G and B unit pixels, wherein at least one unit pixel in the R, G and B unit pixels includes a first transistor and a second transistor, where the first transistor having a first semiconductor layer and the second transistor having a second semiconductor layer and a mobility of the first semiconductor layer is different from a mobility of the second semiconductor layer.

28. The flat panel display according to claim 27, wherein the first semiconductor layer is comprised of an amorphous silicon film, and the second semiconductor layer comprises a polysilicon film.

29. The flat panel display according to claim 27, wherein the first semiconductor layer is comprises of a polysilicon film crystallized by MILC (metal induced lateral crystallization) and the second semiconductor layer comprises a polysilicon film crystallized by MIC (metal induced crystallization).

30. The flat panel display according to claim 27, wherein the first semiconductor layer and the second semiconductor layer are comprised of a polysilicon film crystallized by a sequential lateral solidification (SLS) crystallization method so that of the first semiconductor layer has a crystal grain size that is about 10 times or more smaller than a crystal grain size of the second semiconductor layer, and the first semiconductor layer has a lower mobility than the second semiconductor layer.

31. A flat panel display comprising R, G and B unit pixels, wherein at least one unit pixel in R, G and B unit pixels includes at least a first transistor and a second transistor , wherein the first transistor comprises a first semiconductor layer having a different crystal structure than a crystal structure of a second semiconductor layer of the second transistor.

32. The flat panel display according to claim 31, wherein the first semiconductor layer comprises an amorphous silicon film, and the second semiconductor layer comprises a polysilicon film.

33. The flat panel display according to claim 31, wherein the second semiconductor layer comprises a polysilicon film crystallized by MIC (metal induced crystallization), and the first semiconductor layer comprises a polysilicon film crystallized by MILC.

34. The flat panel display according to claim 31, wherein the first semiconductor layer and the second semiconductor layer are comprised of a polysilicon film crystallized by a sequential lateral solidification (SLS) crystallization method so that a the first semiconductor layer has a grain size that is about 10 times smaller than a grain size of the second semiconductor layer and the first semiconductor layer has a mobility that is lower than a mobility of the second semiconductor layer.